IN THE SPECIFICATION:

The specification as amended below with replacement paragraphs shows added text with underlining and deleted text with ~~strikethrough~~.

Please **REPLACE** the paragraph beginning at page 1, line 6, with the following paragraph:

This application is a Divisional of Application Number 09/532,787, filed March 22, 2000, now pending. The present invention generally relates to microprocessors provided with CPUs, and, more particularly, to a microprocessor which can shorten the period of time required for a chip function test.

Please **REPLACE** the paragraph beginning at page 1, line 11, with the following paragraph:

A microprocessor having a CPU core is normally provided with a bus controller for combining an instruction bus and a data bus into one external bus. The instruction bus and the data bus constitute an internal bus connected to the CPU in the chip. FIG. 15 shows a conventional microprocessor. A CPU 102 which performs arithmetic operations is placed on a microcomputer chip 101. An instruction bus 104 and a data bus 105 which constitute an internal bus extend from the CPU 102, and are combined into one external bus 108 by a bus controller 103. The microprocessor has a ~~brake~~ break mechanism 106 for ~~braking~~ breaking an instruction address. The ~~brake~~ break mechanism 106 ~~comprises~~ includes a plurality of comparators 109 for comparing addresses, and a ~~brake~~ break request generator 110.

Please **REPLACE** the paragraph beginning at page 1, line 27, with the following paragraph:

Each of the comparators 109 compares an address signal supplied from the instruction bus 104 with a signal supplied from the data bus 105 via ~~brake~~ a break point holding register (not shown). A comparison result of each comparator 109 is inputted into the ~~brake~~ break request generator 110. In accordance with the comparison result and a set value of a control register (not shown), the ~~brake~~ break request ~~35~~ generator 110 determines whether or not a

~~brake~~ break request signal should be generated. When generating a ~~brake~~ break request signal, the ~~brake~~ break request generator 110 supplies the ~~brake~~ break signal to the CPU 102 via a signal line 107.

Please **REPLACE** the paragraph beginning at page 4, line 35, with the following paragraph:

FIG. 3 is a block diagram of a ~~brake~~ break mechanism of the microprocessor of FIG. 2;

Please **REPLACE** the paragraph beginning at page 6, line 3, with the following paragraph:

FIG. 2 shows the structure of a microprocessor 1 of this embodiment. The microprocessor 1 is a device which performs arithmetic operations and is formed on a semiconductor chip. The microprocessor 1 comprises a CPU (Central Processing Unit) 2 for performing arithmetic operations, a bus controller 3 for combining an internal instruction bus 4 and an internal bus 8, a ~~brake~~ break mechanism 6 for ~~braking~~ breaking an instruction address, and a test circuit 10 which generates test addresses in ~~an~~ a function to shorten the testing period of time.

Please **REPLACE** the paragraph beginning at page 6, line 27, with the following paragraph:

FIG. 3 shows the inner structure of the ~~brake~~ break mechanism 6. As shown in this figure, a plurality of ~~brake~~ break point holding registers 21 to 23 are connected to the internal data bus 5, and each hold a value supplied from the internal data bus 5. Although only the three ~~brake~~ break point holding registers 21 to 23 are shown in FIG. 3, more ~~of then~~ can be employed. The output signals of the ~~brake~~ break point holding registers are supplied to three comparators 26 to 28, respectively. Like the ~~brake~~ break point holding registers 21 to 23, the number of comparators is not necessarily three. The other input terminals of the comparators 26 to 28 are connected to the internal instruction bus 4. Each of the comparators 26 to 28 compares an address value supplied from the internal instruction bus 4 with a value supplied from the internal data bus 5 via each corresponding ~~brake~~ break point holding resistor 21, 22, or 23. If the two values are identical, the comparison result is supplied to a ~~brake~~ break request generator 25.

The break request generator 25 is connected to a control register 24 also connected to the internal bus 5. In accordance with a control signal supplied from the control register 24, the ~~brake~~ break request generator 25 determines whether it should output a ~~brake~~ break request to the CPU 2.

Please **REPLACE** the paragraph beginning at page 7, line 16, with the following paragraph:

In the ~~brake~~ break mechanism 6 having the above structure, the comparators 26 to 28 compare addresses, and output a ~~break~~ break request in accordance with the comparison result. The ~~brake~~ break request is supplied to the CPU 2 via a signal line 7. In this embodiment, ~~an~~ a function test is conducted to check whether or not the comparators 26 to 28 in the ~~brake~~ break mechanism 6 operate properly. More specifically, a test address generated by the test circuit 10 is supplied to the comparators 26 to 28, and ~~an~~ a function test is carried out in a short period of ~~tome~~ time. In the function test, a signal line 13 branching out from the signal line 7 is used to output a test result supplied from the ~~brake~~ break mechanism 6.

Please **REPLACE** the paragraph beginning at page 7, line 31, with the following paragraph:

The test circuit 10 is connected to the internal data bus 5, so that a value from the internal data bus 5 is inputted into the test circuit 10. The test circuit 10 is also connected to the internal instruction bus 4 via a signal line 11, so that the test circuit 10 outputs a test address to the internal instruction bus 4. The test circuit 10 is also connected to the CPU 2 via a signal line 12 to output a signal to the CPU 2. The signal line 12 is used to output a signal for providing high impedance to a terminal connected to the internal instruction bus 4 during the function test. This terminal is located in the CPU 2. In the function test, the CPU 2 frees the internal instruction bus 4, so that the internal instruction bus 4 receives a test address from the test circuit 10. The test address is then supplied to each of the comparators 26 to 28 of the ~~brake~~ break mechanism 6.

Please **REPLACE** the paragraph beginning at page 8, line 12, with the following paragraph:

In the function test, the test circuit 10 generates various test addresses. To generate test addresses, any of known techniques can be employed. For instance, a memory table or registers can be used to generate test addresses, or a control technique illustrated in FIG. 4 can be employed. The test circuit 10 supplies test addresses to each of the comparators 26 to 28. In accordance with the test addresses, each of the comparators 26 to 28 supplies a signal to the ~~brake~~ break request generator 25. In the function test, the signal line 13 branching out from the signal line 7 is used for transmitting the output from the ~~brake~~ break request generator 25. The signal line 13 is allocated to an external terminal of the microprocessor 1, and outputs a test result through the external terminal. Accordingly, whether a test result corresponding to the test addresses generated by the test circuit 10 is obtained can be determined by monitoring the external terminal connected to the signal line 13. During the function test, the CPU 2 stops executing the program. By doing so, the comparators 26 to 28 can be ~~test~~ tested, with the CPU 2 executing no instruction. For instance, one comparator testing operation can performed per clock.

Please **REPLACE** the paragraph beginning at page 11, line 37, with the following paragraph:

When the bus driver 36 starts controlling the internal instruction bus 4, a test address generated within the bit pattern register 35 is outputted to the bus driver 36, and is further transferred to the instruction address bus 4a. At the same time, an instruction read signal is switched to a signal indicating that an instruction should be fetched in accordance with a signal from the bus driver 36. The instruction read signal is then supplied to all the slaves connected to the 10 instruction address bus 4a. When the instruction read signal is switched, a test address supplied to the instruction address bus 4a is sent to one of the input terminals of each of the comparators 26 to 28. Here, the values held in the ~~brake~~ break point holding registers 21 to 23 are compared with the test address supplied from the test circuit, and the comparison result is outputted to the ~~brake~~ break request generator 25. At this point, in compliance with the bus release request signal from the test circuit 10, the CPU 2 ignores the ~~brake~~ break request signal from the ~~brake~~ break request generator 25. As a result, the signal including the test result supplied from the ~~brake~~ break request generator 25 is outputted through the signal the line 13 to the outside of the chip. The conditions of the comparators 26 to 28 in the ~~brake~~ break

mechanism 6 can be determined by monitoring the signal outputted through signal line 13. Since the CPU 2 does not execute the program after the start of the test circuit 10, a very high-speed test can be carried out.

Please **REPLACE** the paragraph beginning at page 13, line 13, with the following paragraph:

If the rotator 34 rotates to shift address value of the bit pattern register 35 by 1 bit, 32 test addresses are generated for a 32-bit microprocessor 6, and the comparison test is carried out for each of the comparators in the ~~brake~~ break mechanism 6. After the test, the test circuit 10 ~~is~~ changes the bus release request signal level on the signal line 12, and notifies the CPU 2 of the completion of the test. As a result, the CPU 2 releases its connection portions with the internal instruction bus 4 from the high-impedance state, and resumes executing the program.

Please **REPLACE** the paragraph beginning at page 14, line 13, with the following paragraph:

A microprocessor 41 of this embodiment contains a test result holding register 42. As shown in FIG. 5, the microprocessor 41 of this embodiment ~~comprises~~ includes the CPU 2 which carries out certain arithmetic operations, a bus controller 3 which combines the internal instruction bus 4 and the internal data bus 5 into the single external bus 8, the ~~brake~~ break mechanism 6 which includes the comparators to be tested and ~~brakes~~ breaks an instruction address, the test circuit which generates predetermined test addresses during ~~an~~ a function test, and the test result holding register 42 which holds test results. The CPU 2, the internal instruction bus 4, the internal data bus 5, the bus controller 3, the ~~brake~~ break mechanism 6, and the test circuit 10 are the same as in the first embodiment.

Please **REPLACE** the paragraph beginning at page 14, line 29, with the following paragraph:

The test result holding register 42 is connected to the signal line 13 branching out from the signal line 7 extending from the ~~brake~~ break mechanism 6 to the CPU 2. The test result holding register 42 temporarily holds test results, and outputs the results after ~~an~~ a function test is completed and the CPU 2 resumes executing the program. The test result holding register 42

is connected so that it can exchange data with the internal data bus 5.

Please **REPLACE** the paragraph beginning at page 16, line 5, with the following paragraph:

As in the first embodiment, ~~an~~ a function test of each of the comparators (not shown) in the ~~brake~~ break mechanism 6 is carried out in accordance with test addresses generated by the test circuit 10. At this point, the internal instruction bus 4 is in a released state, and the CPU 2 is not executing the program. During each function test, the test addresses are sequentially supplied from the test circuit 10 to the comparators in the ~~brake~~ break mechanism 6 via the internal instruction bus 4. In this embodiment, an expected value which is expected to be outputted when a comparator is properly operating is inputted for comparison from the external bus 8 into the comparison result determination circuit 45 via the bus controller 3 and the internal data bus 5 in synchronization with the supply of the test addresses. The comparison result determination circuit 45 compares the expected value with each actual test result, i.e., if the actual test result indicates that the comparator is defective, the comparison result determination circuit 45 supplies a signal to the flag register 43 so as to set the flag in the flag register 43 to "1". If the actual test results are identical to the respective expected values in all the bit patterns at the test addresses, i.e., if the actual test results ~~indicates~~ indicate that all the comparators have no defects, the comparison result determination circuit 45 sends no signal to the flag register 43, so that the flag in the flag register 43 is maintained at "0". Especially, since the internal operating frequency is sufficiently higher than the external operating frequency, ~~it is preferable to perform~~ a comparison operation on a plurality of bits inputted from the outside of the chip is performed, instead of performing a comparison operation on one bit at a time. Therefore, a plurality of expected values are collectively inputted so as to facilitate the comparison operations.

Please **REPLACE** the paragraph beginning at page 18, line 8, with the following paragraph:

As shown in FIG. 7, the microprocessor 51 of this embodiment comprises the CPU 52 which performs certain arithmetic operations, a bus controller 53 which combines an internal instruction bus and the internal data bus 5 into the single external bus 8, the ~~brake~~ break mechanism 6 which ~~brakes~~ breaks an instruction address via the signal line 7, and the test

circuit 54 which generates predetermined test addresses during ~~an~~ a function test so as to shorten the testing period. The ~~brake~~ break mechanism 6, the internal data bus 5, and the external bus 8 are the same as in the first and second embodiments.

Please **REPLACE** the paragraph beginning at page 18, line 20, with the following paragraph:

In the microprocessor 51 of this embodiment, a data bus 55, an address bus 56, and read signal lines 57 and 58 constitute an internal instruction bus. The data bus 55 is used when the CPU 52 fetches an instruction. The address bus 56 transmits the address of each instruction. Since each of the comparators in the ~~brake~~ break mechanism 6 compares addresses, the ~~brake~~ break mechanism 6 is connected to the address bus 56. In an function test, each of the comparators is tested based on the test addresses supplied from the CPU 52. The read signal lines 57 and 58 transmit an instruction read signal from the CPU 52. When the instruction read signal switches its status, the timing for fetching an instruction is transmitted to each circuit.

Please **REPLACE** the paragraph beginning at page 19, line 23, with the following paragraph:

The operation of the test circuit 54 will now be described. Assuming that the microprocessor 51 is in an initial state after its production, the CPU 52 starts to execute its program. When the CPU 52 switches to ~~an~~ a function test in accordance with the program, the CPU 52 transmits a branch generation signal via the signal line 59 to notify the test circuit 54 of the first branch generation, thereby activating the test circuit 54. As the test circuit 54 is activated, the CPU 52 repeats branching by a call instruction CALL so as to carry out the test on the comparators in the ~~brake~~ break mechanism 6. In the branching by the call instruction CALL, the CPU 52 can send a desired test address to the ~~brake~~ break mechanism 6. When the CPU 52 switches the read signal to repeat the instruction fetch, the test circuit 54 masks the read signal on the signal line 57 against the signal line 58, and transmits a return instruction RET via the signal line 60. By this signal replacing operation of the test circuit 54, the CPU 52 can certainly return to the original program whether or not a program exists at a test address after branching. Thus, the CPU 52 can be prevented from overrunning.